

CLAIMS

1. An integrated circuit comprising a buried layer of determined conductivity type in a plane substantially parallel to the plane of a main circuit surface, wherein a median portion of said buried layer is filled with a metal-type material.

5 2. The integrated circuit of claim 1, wherein the buried layer is a sub-collector layer of a bipolar transistor.

3. The integrated circuit of claim 1, wherein the metal-type material is titanium nitride.

10

4. A method for forming a buried layer in a semiconductor substrate of an integrated circuit, comprising the steps of:

providing, at the location where the buried layer is to be formed, a layer portion made of a material selectively etchable with respect to the rest of the semiconductor material,

15

doping the semiconductor substrate according to a chosen conductivity type on either side of said layer portion,

digging an opening extending from the integrated circuit surface to said layer portion,

20

removing said layer portion by isotropic etch, and

filling the cavity thus formed with a metal-type material.

5. The method of claim 4, wherein the layer portion is delimited by an insulating wall.

25

6. The method of claim 4, wherein the layer portion is a silicon-germanium region formed by epitaxy on a silicon substrate and itself covered with a silicon epitaxial layer.

30

7. The method of claim 4, wherein the layer portion is a silicon oxide region, formed on a silicon substrate and coated with a silicon layer.

8. The method of claim 4, wherein the layer portion is a hollowed region formed in advance in the semiconductor substrate.